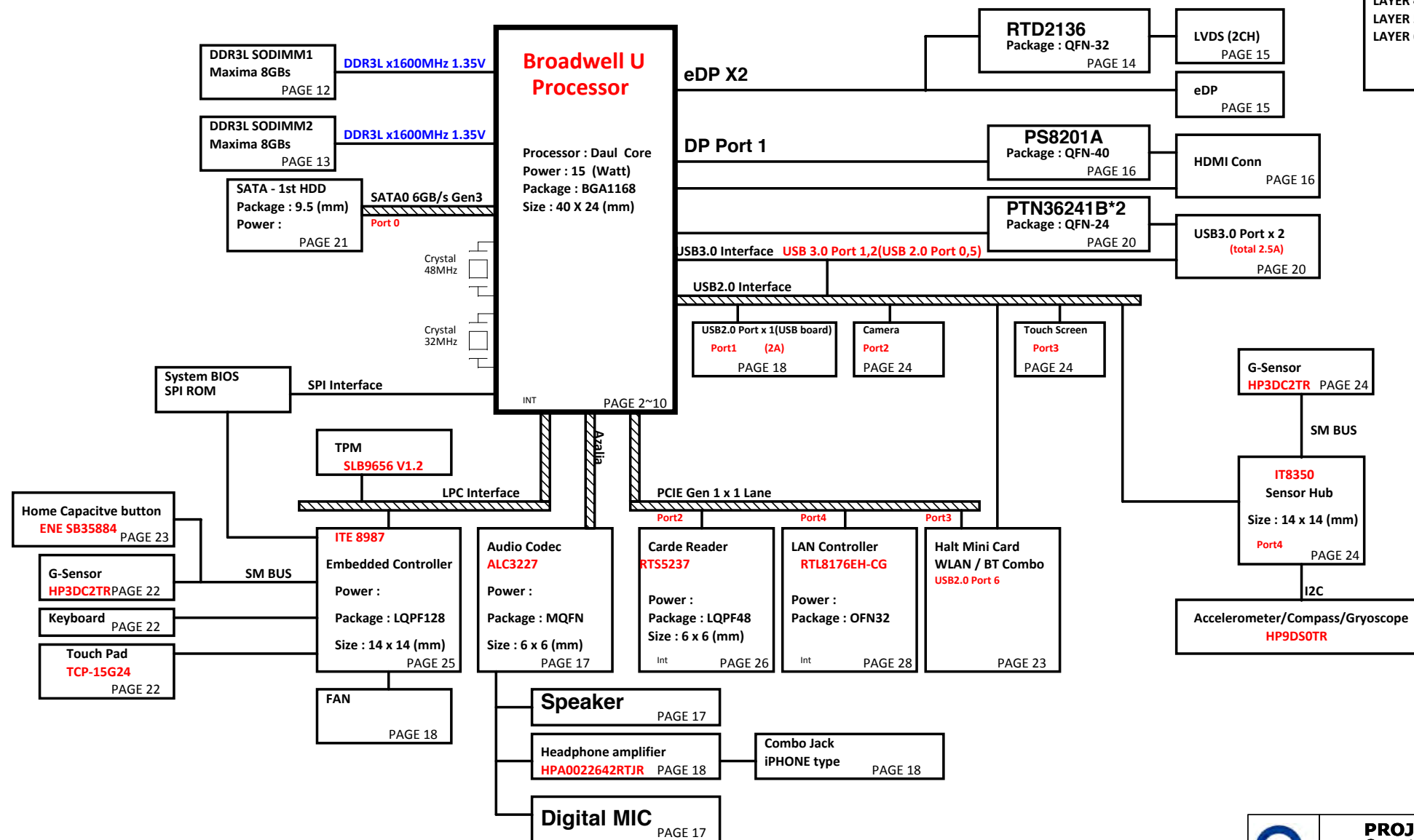


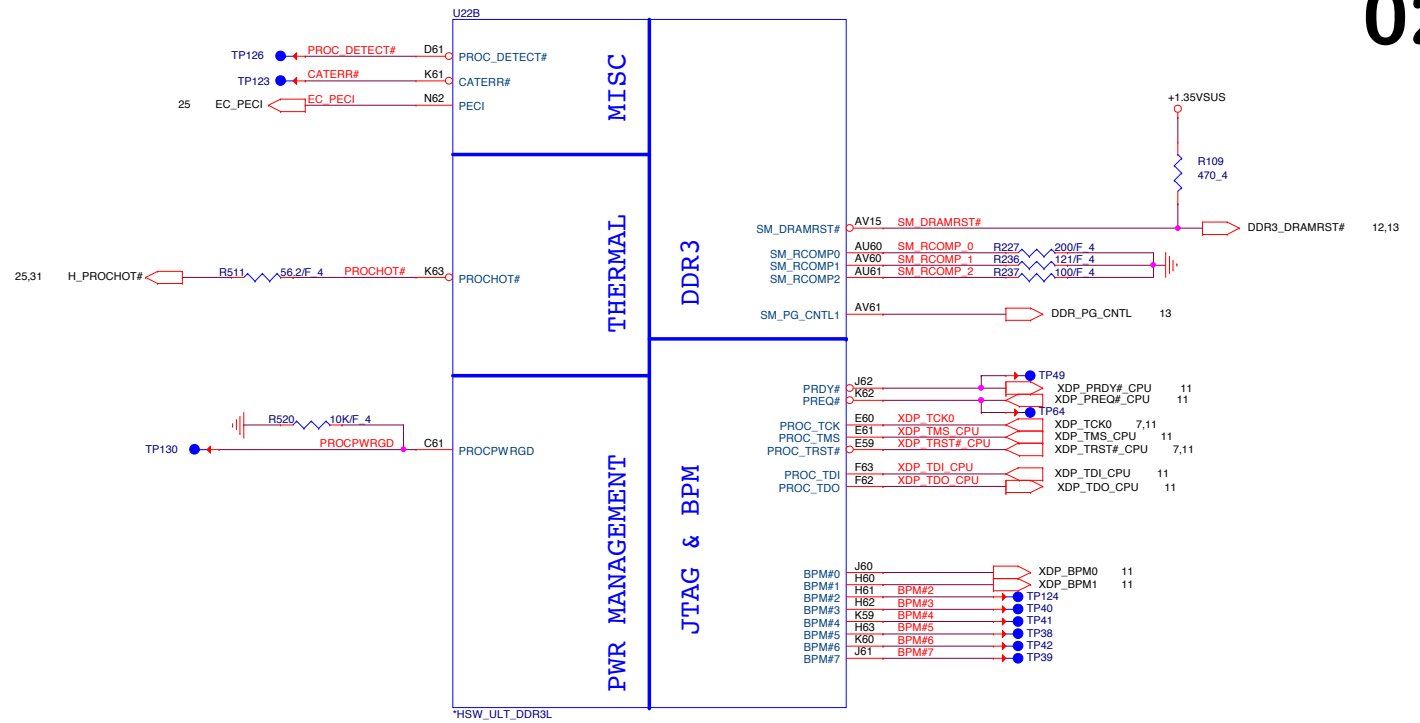
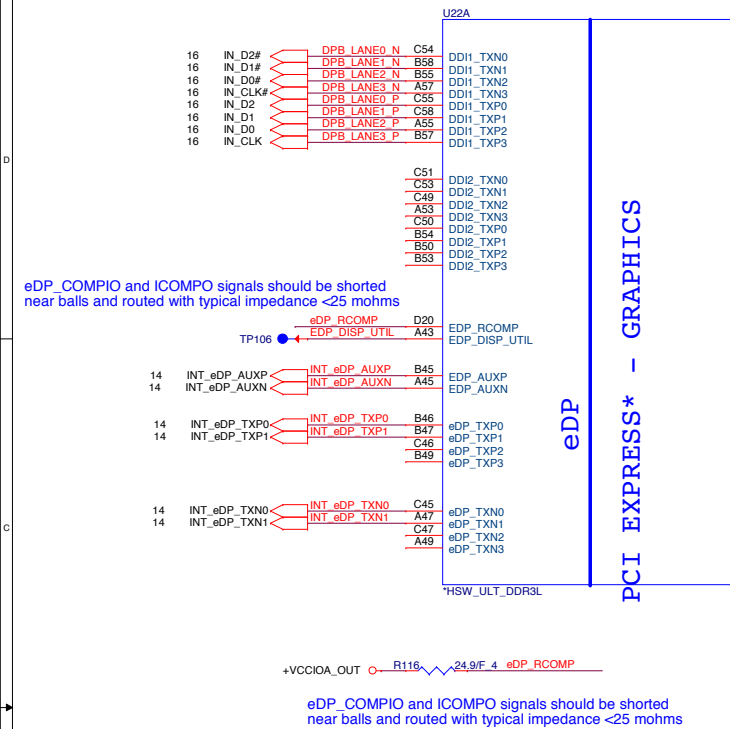
13"/15"

Y61 Intel Cresnet Bay ULT Platform Block Diagram

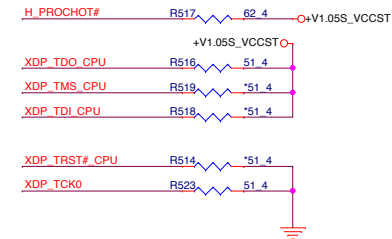
PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

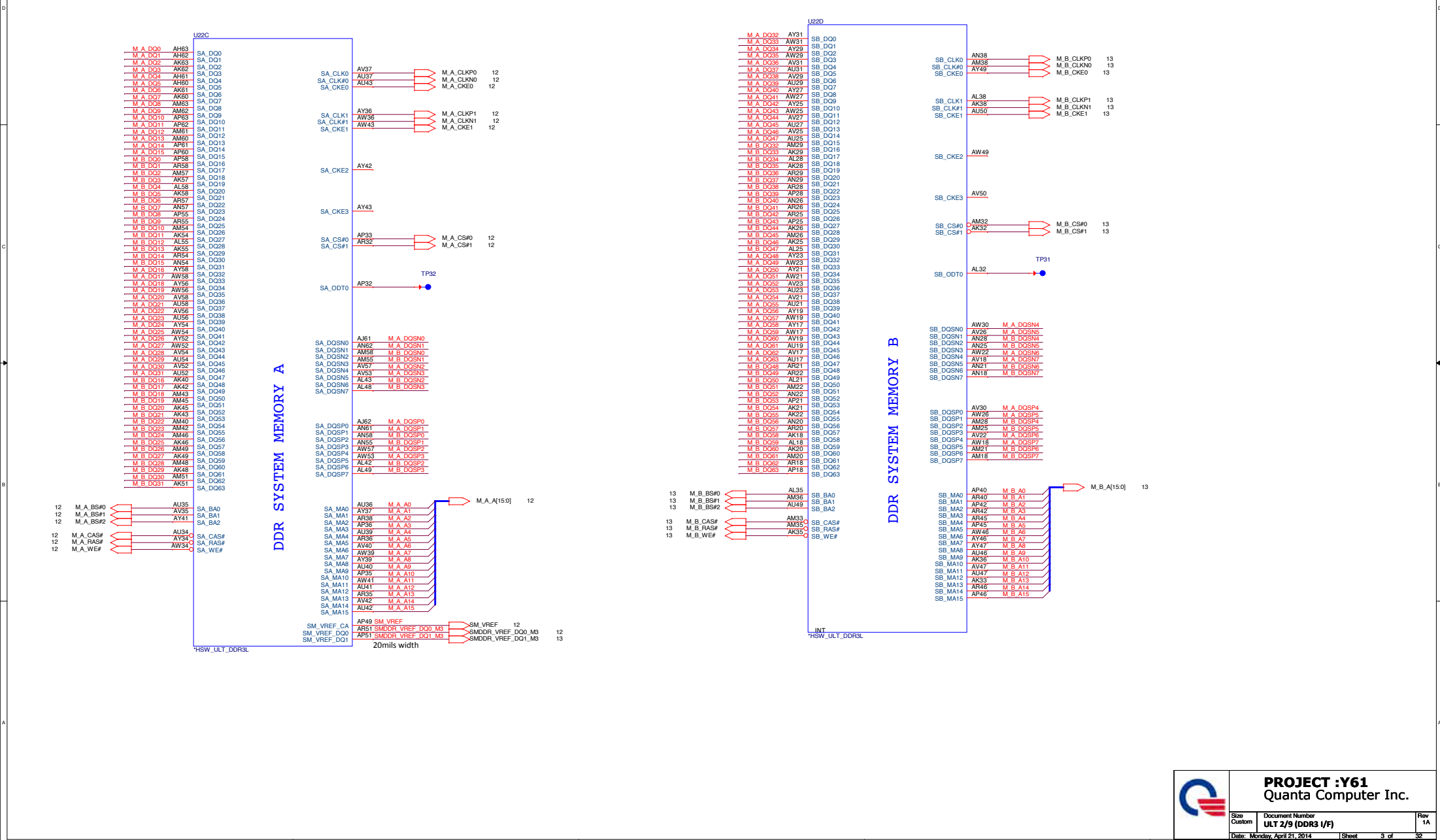


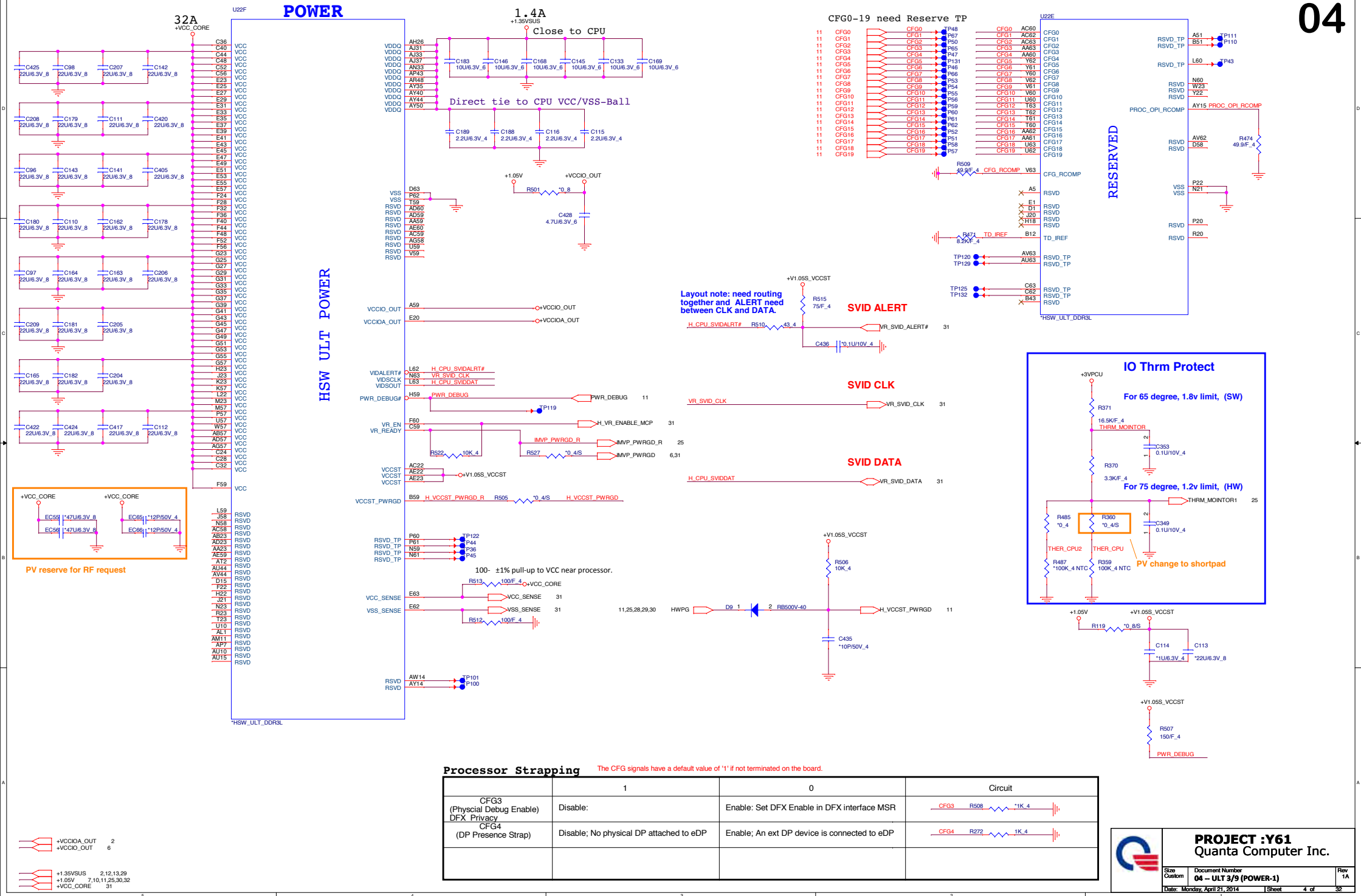


Processor pull-up (CPU)

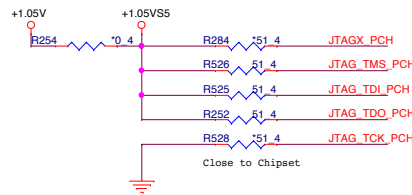


Haswell ULT Processor (DDR3L)

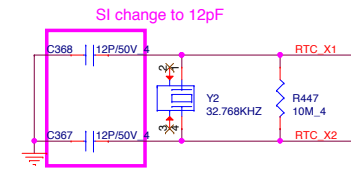




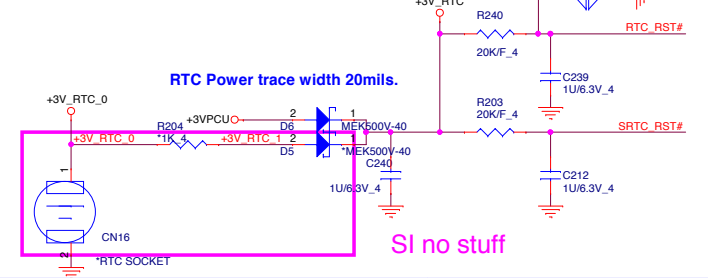
07



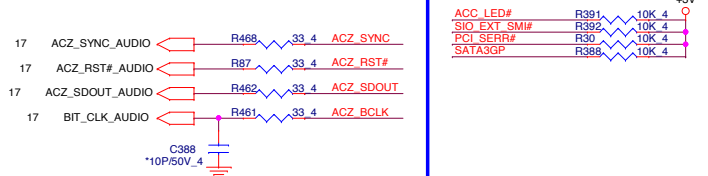
RTC Clock 32.768KHz



30mils

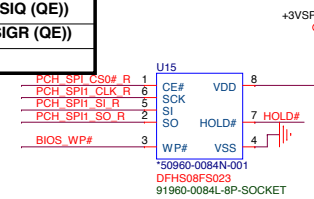


GPIO Pull UP

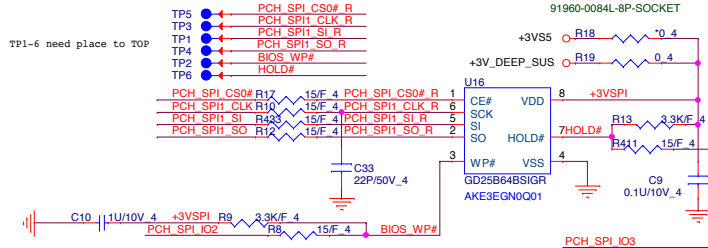


Vender	Size	P/N
EON	8MB	AKE3EZ2N0Q01 (EN25QH64-104HIP (QE
Winbond	8MB	AKE3EFPN07 (W25Q64FVSSIQ (QE))
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR (QE))
Socket		DFHS08FS023

4M SPI ROM Socket



PCH SPI ROM(CLG)

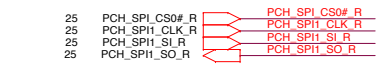


PROJECT :Y61
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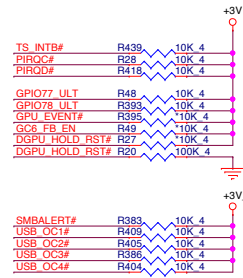
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden							
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"><thead><tr><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>LPC</td></tr><tr><td>0</td><td>SPI(Default)</td></tr></tbody></table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)	
GNT0#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up							

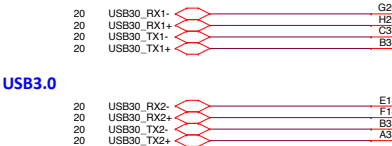


Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

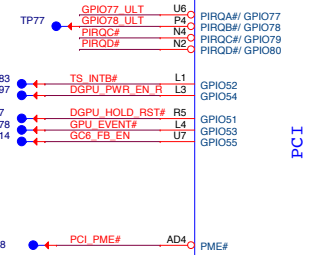
PCI/USBOC# Pull-up(CLG)



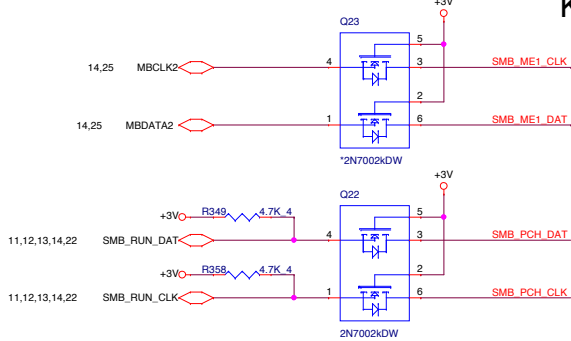
USB3.0



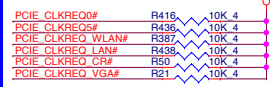
PCI



SMBus/Pull-up(CLG)



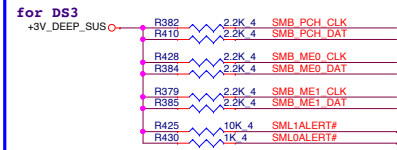
K501UB



CLK_REQ/Strap Pin(CLG) +3



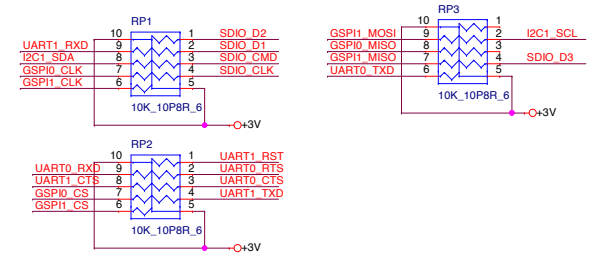
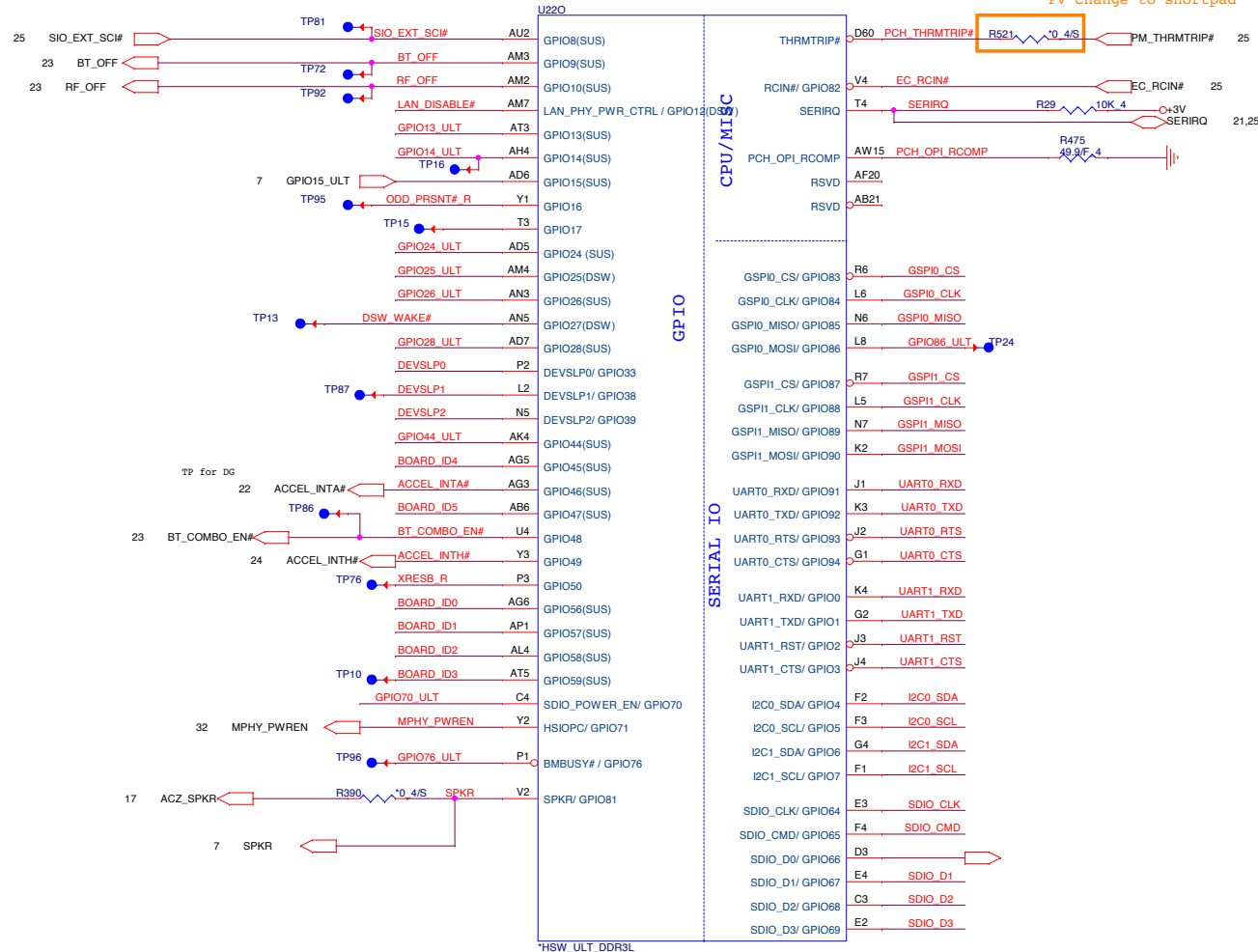
SMBus/Pull-up(CLG)



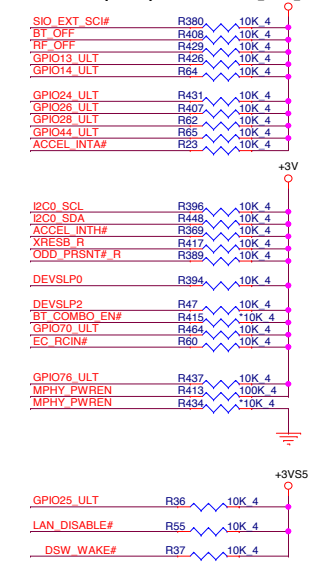
PROJECT :Y61
Quanta Computer Inc.

Size Custom	Document Number ULT 7/9 (PCIE/USB/CLK)	Rev 1A
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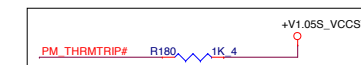
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)



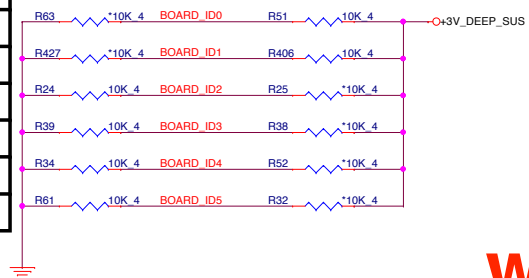
GPIO Pull-up/Pull-down(CLG)



Close to EC



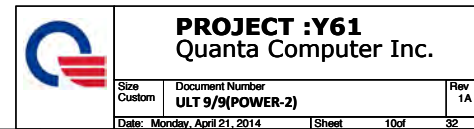
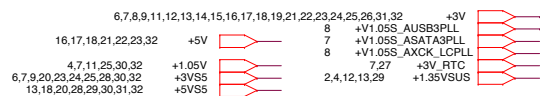
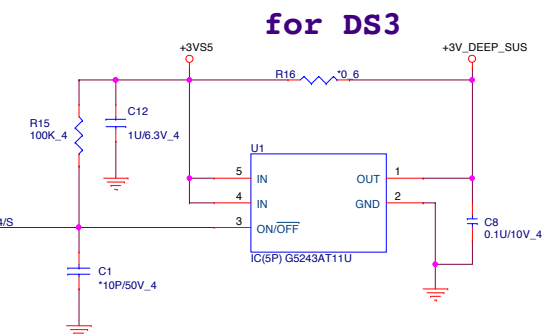
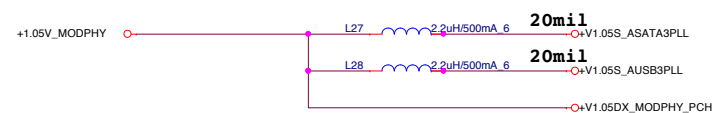
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
13" clamshell wo/TS	0	0	0	0	0	1
13" convertible w/TS	0	0	0	0	1	0
15" convertible w/TS+ Giga NIC	0	0	0	0	1	1
13" clamshell w/TS (Reserve)	0	0	0	0	0	0
13" convertible wo/TS (Reserve)	0	0	0	0	0	0
15" convertible w/TS (Reserve)	0	0	0	0	0	0

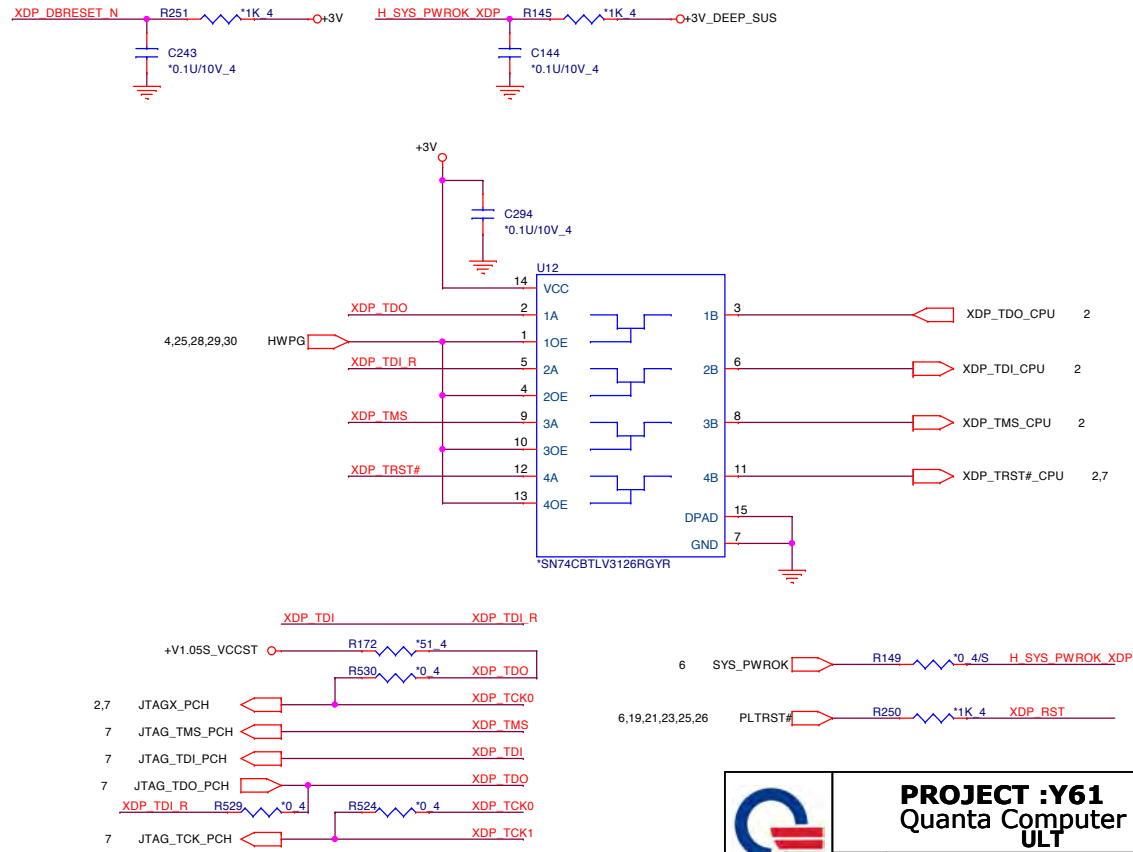
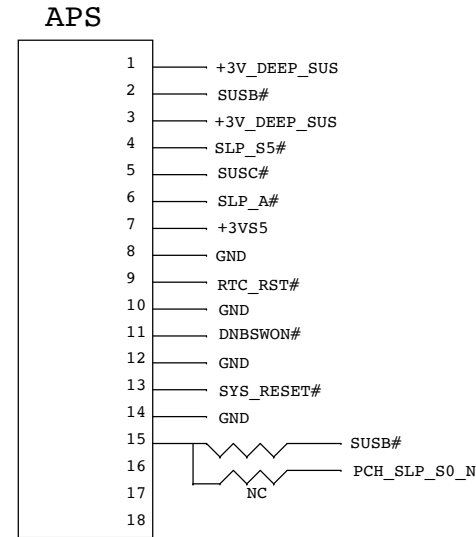
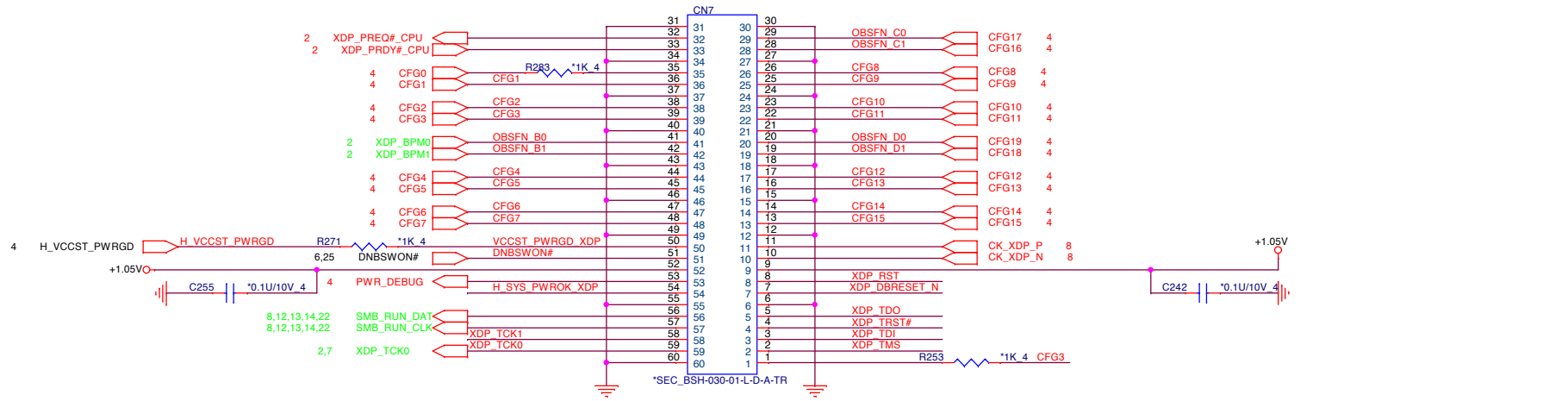


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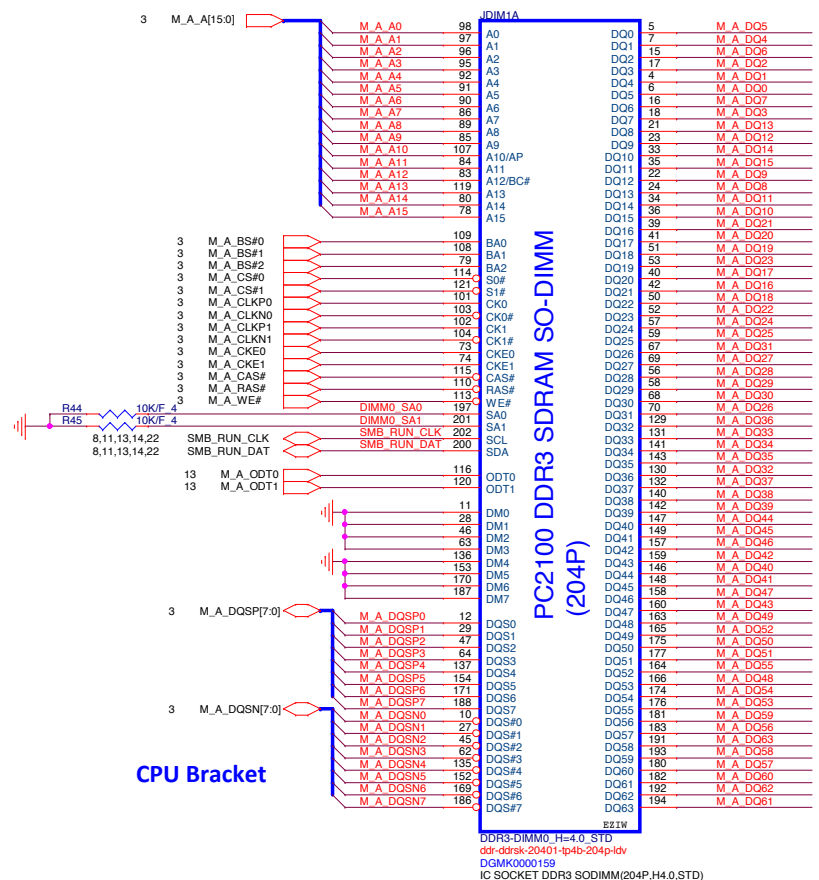
PROJECT :Y61
Quanta Computer Inc.

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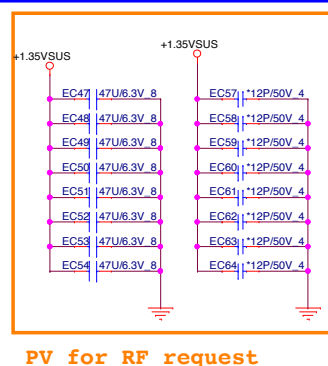
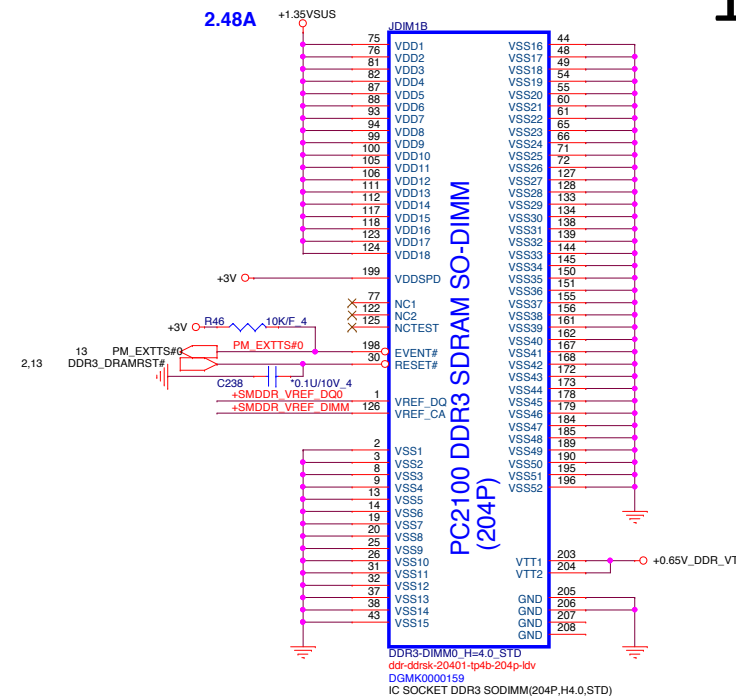




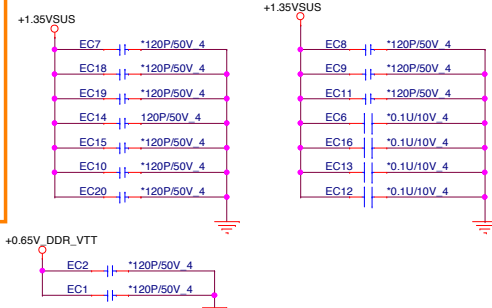
PROJECT :Y61
Quanta Computer Inc.
ULT



M_A_DQ[63:0] 3

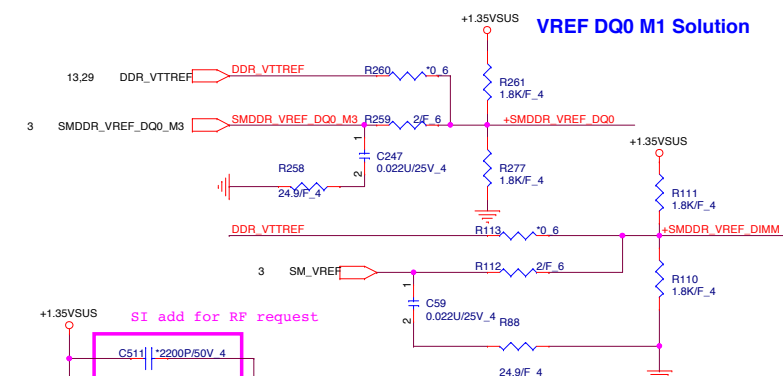
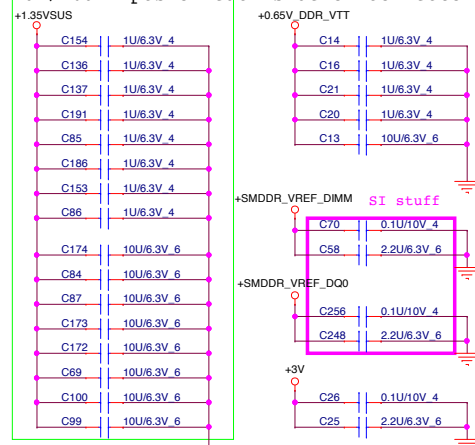


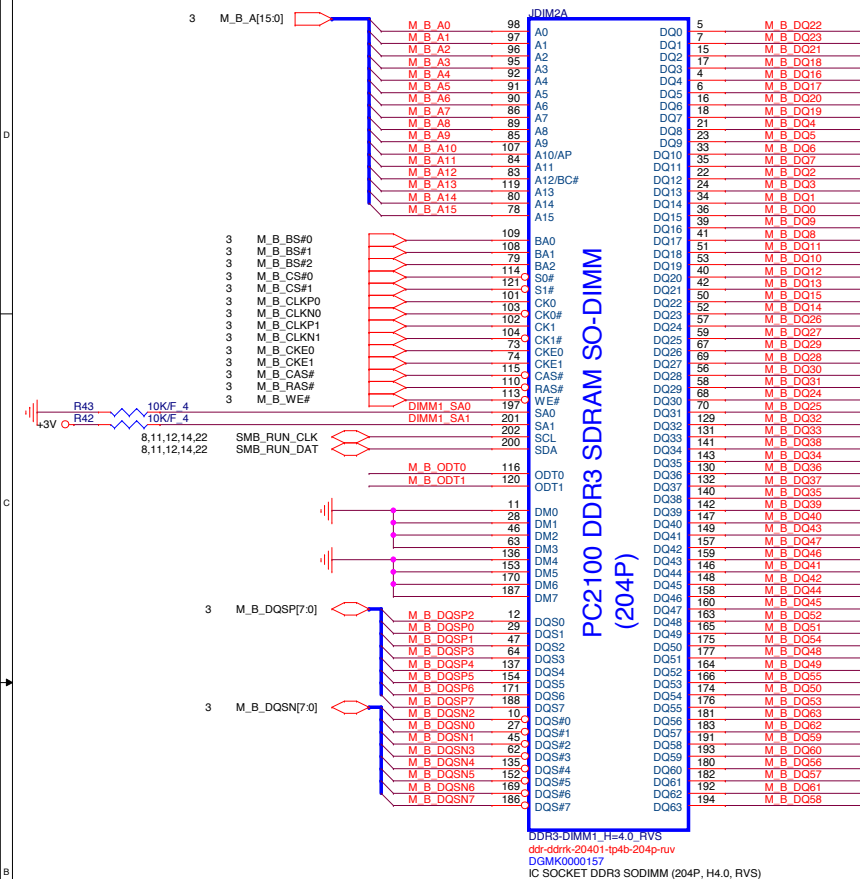
For EMI RESERVE

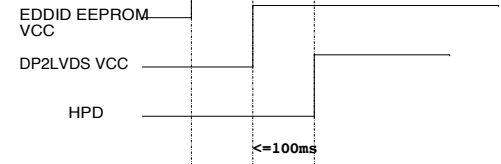


Place these Caps near So-Dimm0.

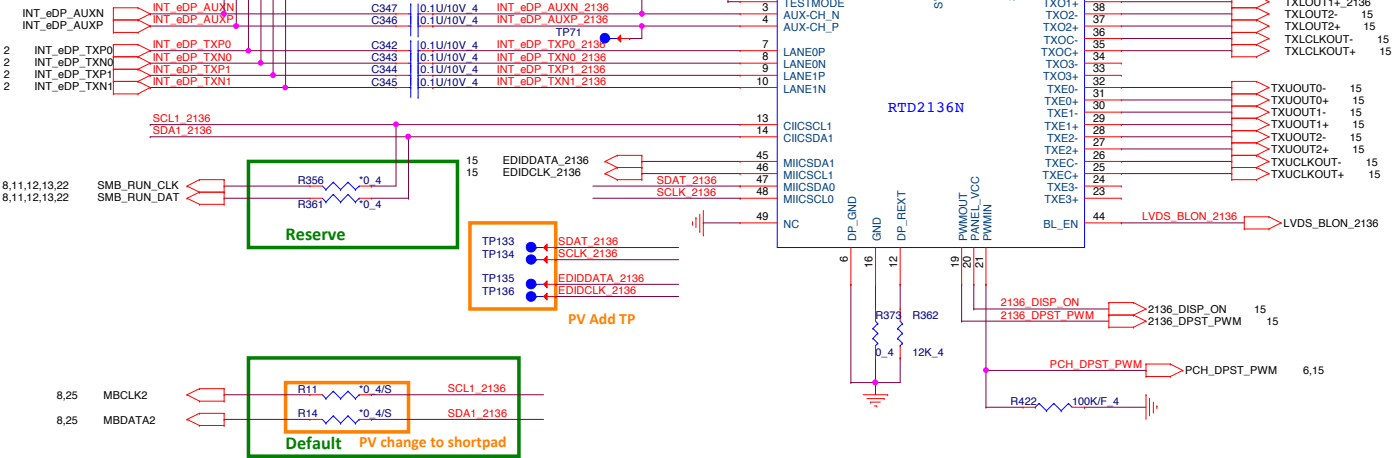
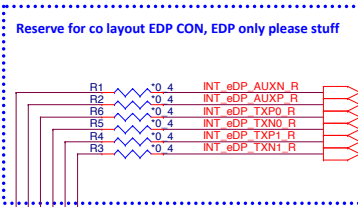
1uF/10uF 4pcs on each side of connector



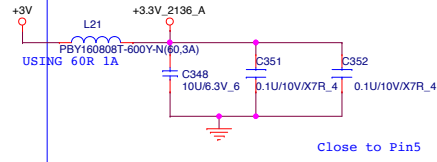
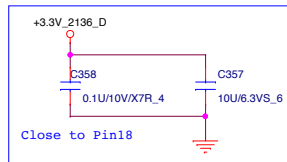
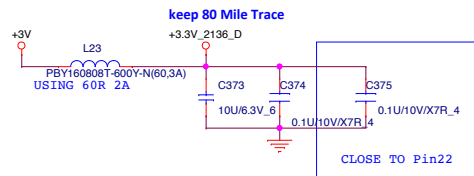
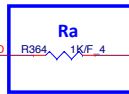




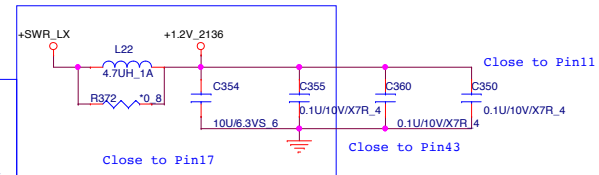
PV remove EEPROM



For EDP: unstuff Ra



L110: need use CV-4709MN00 for Vendor suggestion

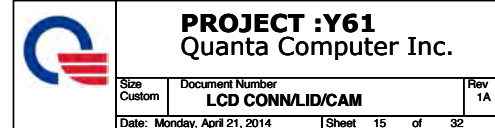
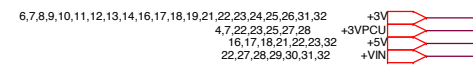
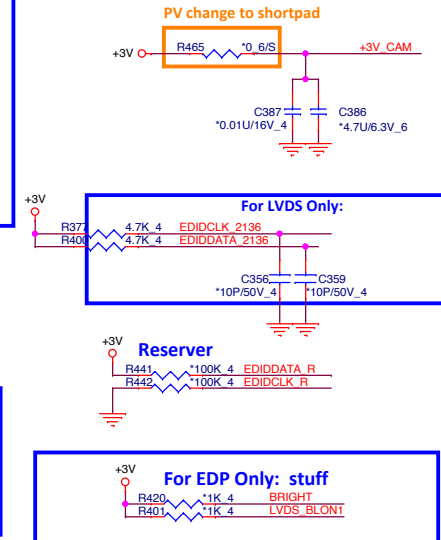
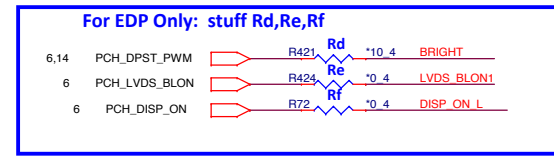
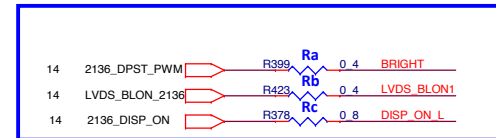
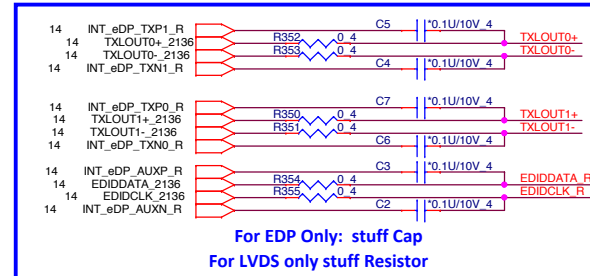
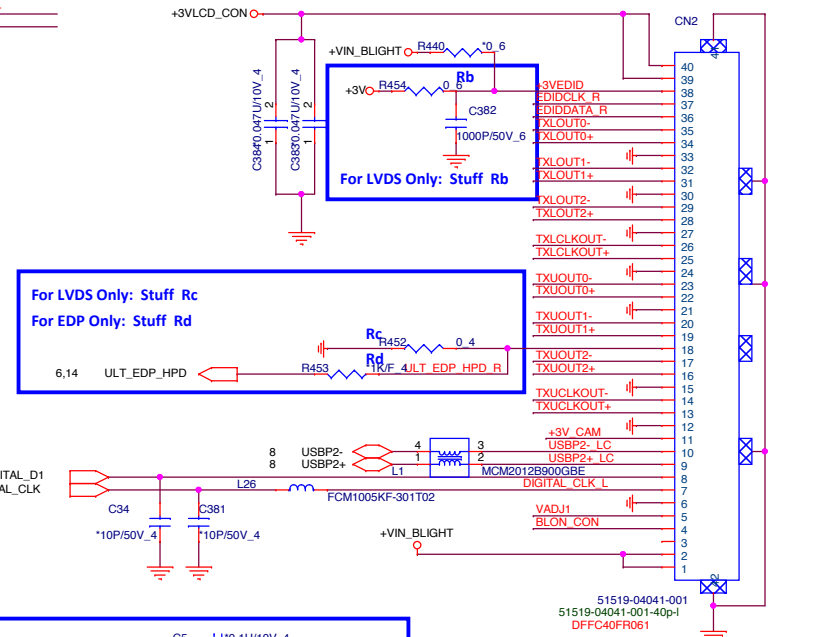
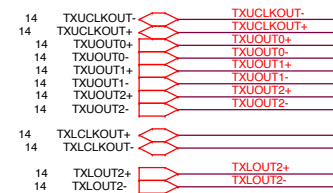
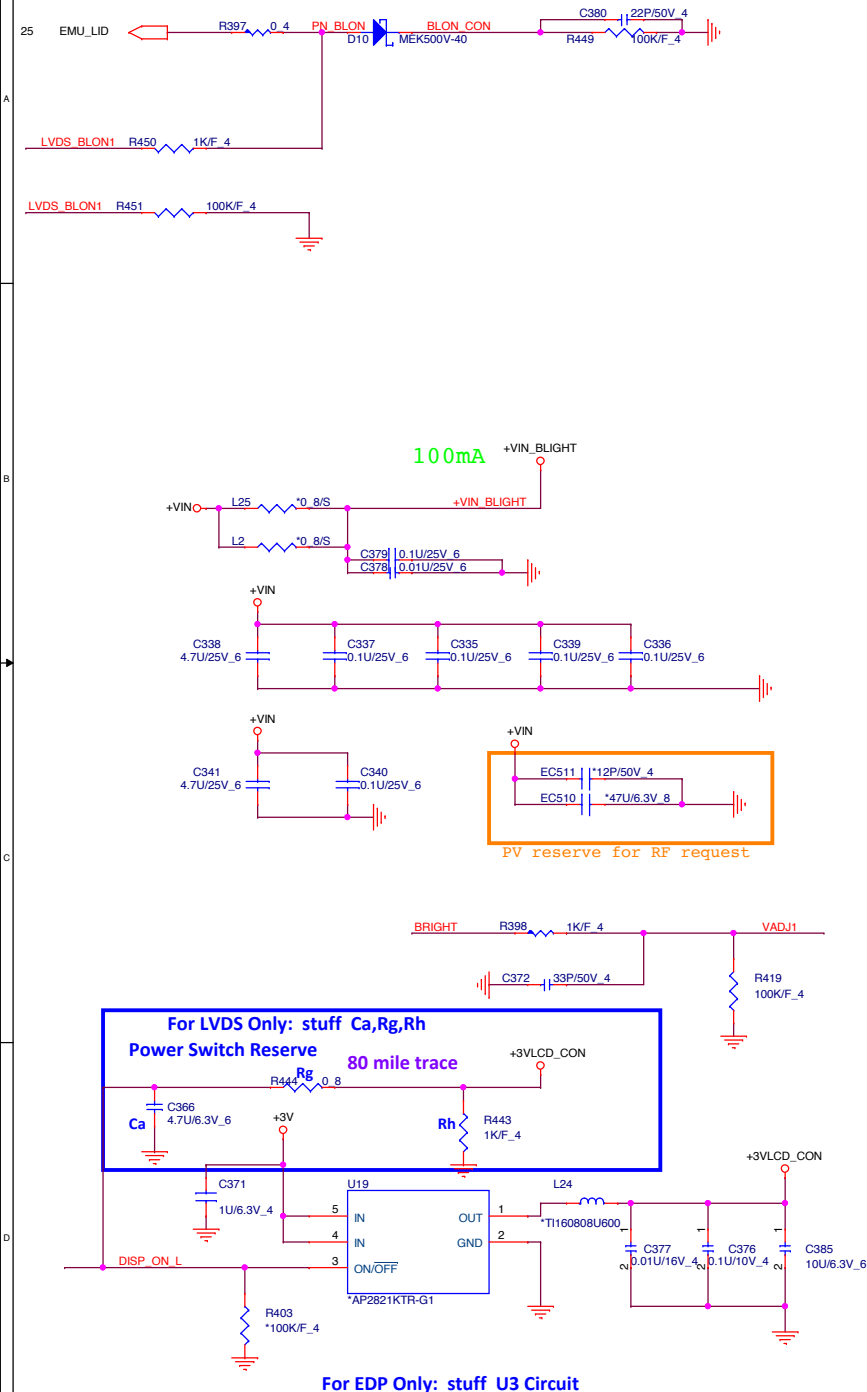


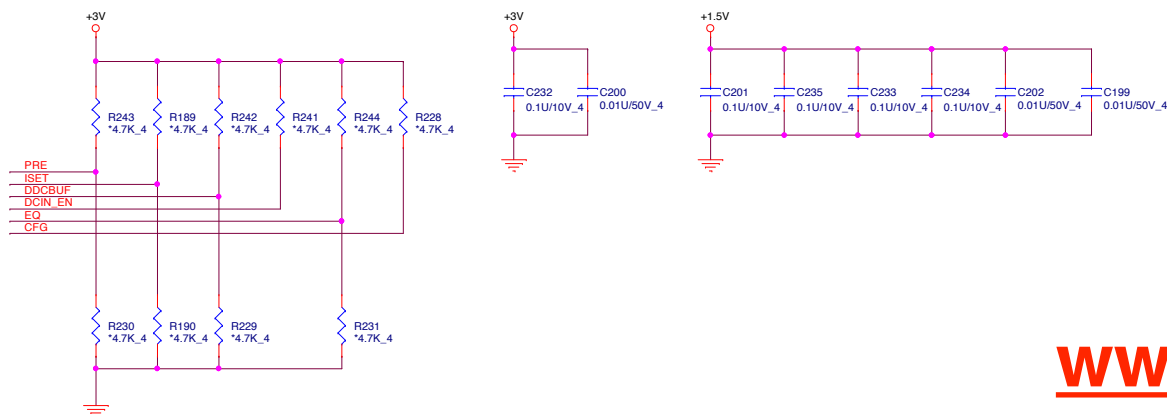
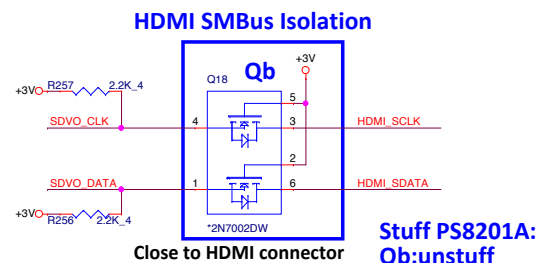
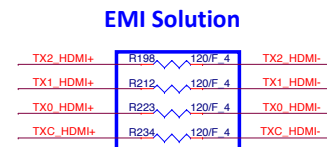
SWR MODE	LDO MODE
Stuff L22	Stuff R372

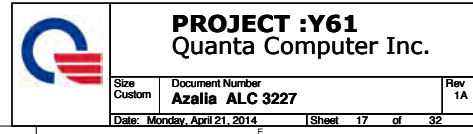
LID Switch

LVDS Conn.

15

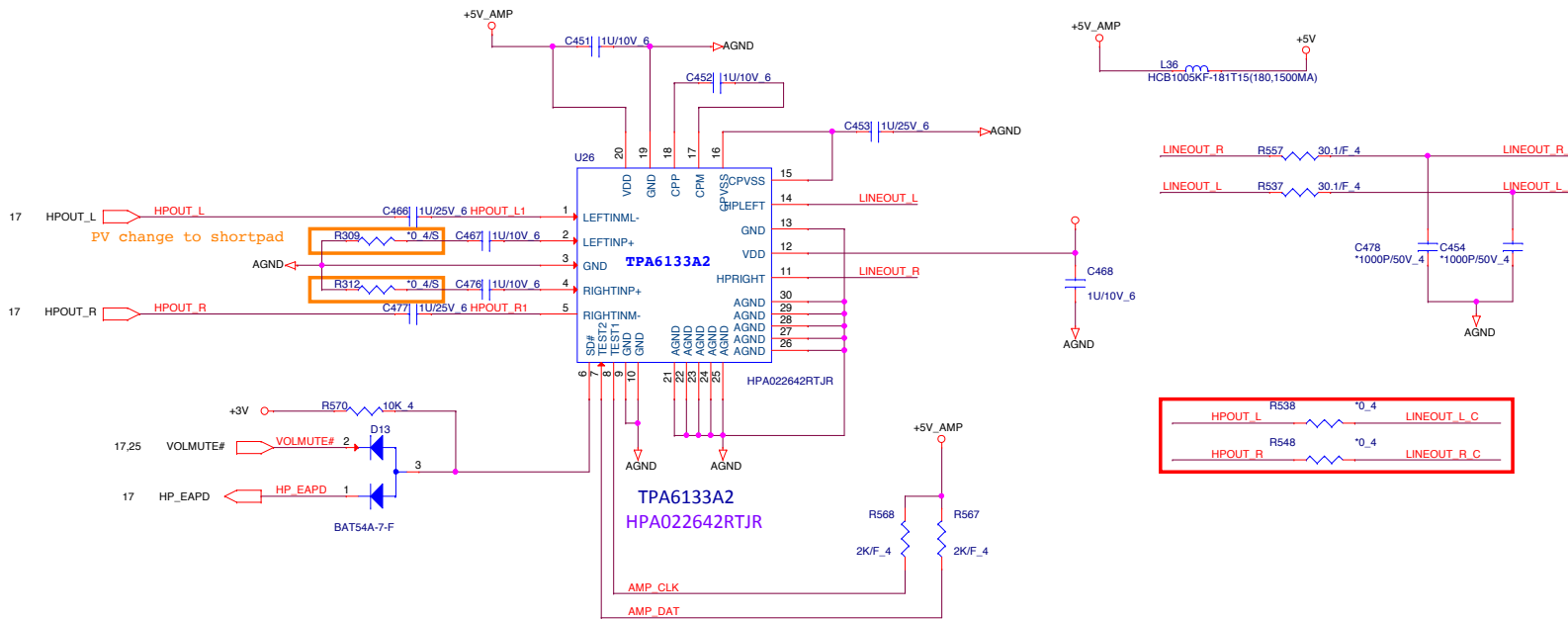




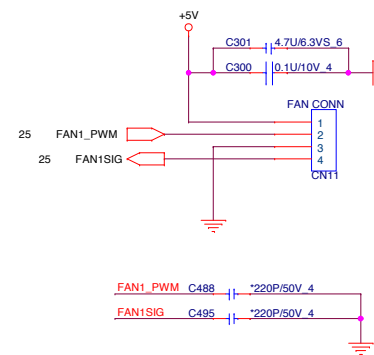


Head Phone out

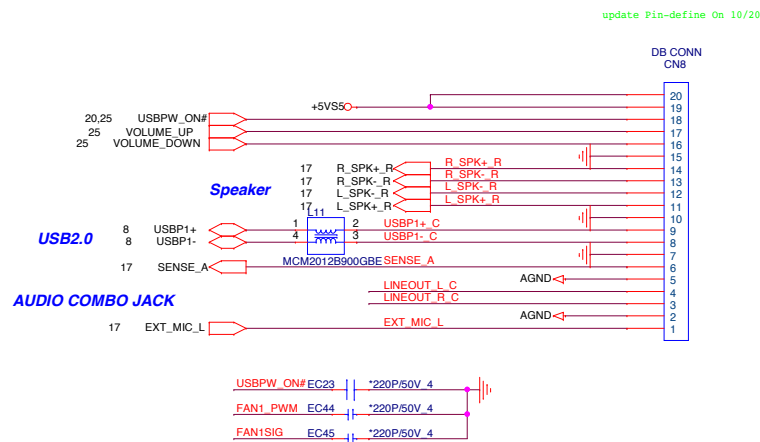
18



FAN



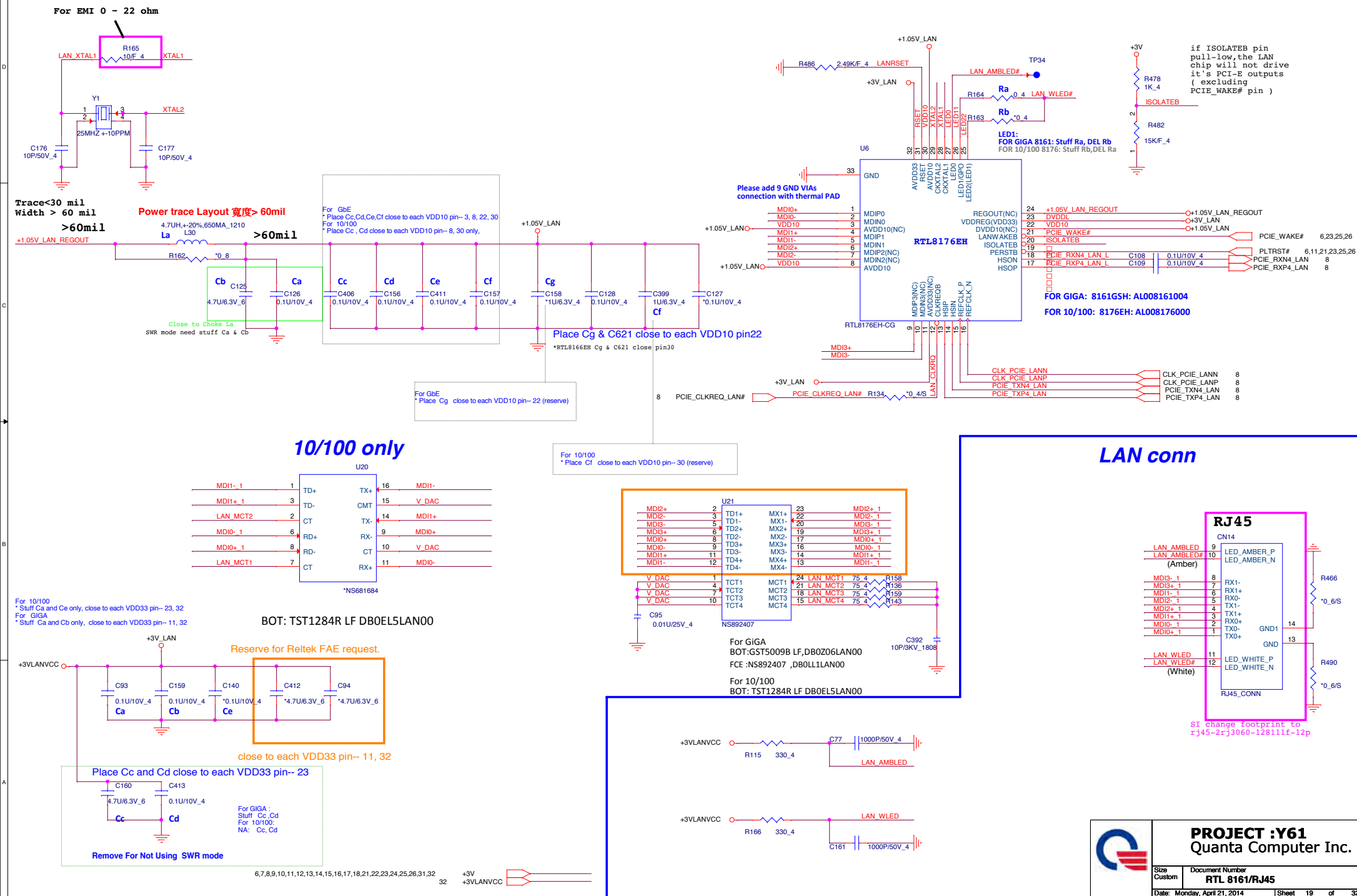
Audio Board



6,7,8,9,10,11,12,13,14,15,16,17,19,21,22,23,24,25,26,31,32
16,17,21,22,23,32
13,20,28,29,30,31,32

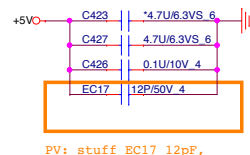
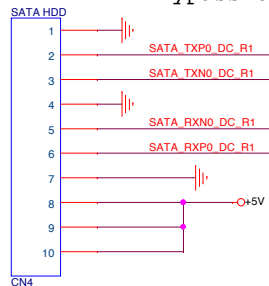
+3V
+5V
+5VSS

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SATA HDD Connector(Cable type)

Bypass CAP close conn



PV: stuff EC17 12pF,

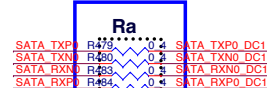
SI add for co-lay use

SATA_TXP0_DC_R1	R584	0.4	SATA_TXP0_DC_R
SATA_TXN0_DC_R1	R586	0.4	SATA_TXN0_DC_R
SATA_RXN0_DC_R1	R585	0.4	SATA_RXN0_DC_R
SATA_RXP0_DC_R1	R587	0.4	SATA_RXP0_DC_R
SATA_TXP0_DC_R2	R589	0.4	SATA_TXP0_DC_R
SATA_TXN0_DC_R2	R591	0.4	SATA_TXN0_DC_R
SATA_RXN0_DC_R2	R588	0.4	SATA_RXN0_DC_R
SATA_RXP0_DC_R2	R590	0.4	SATA_RXP0_DC_R

SATA Re-driver

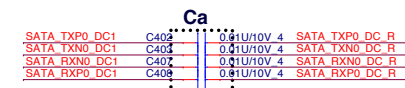
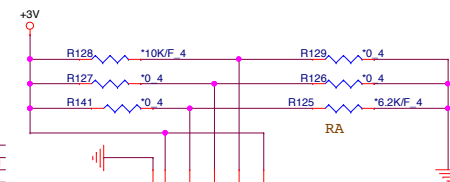
Ra & Rb need place close

HOST



Ra

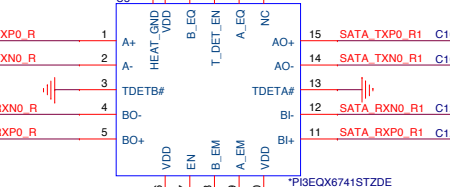
Rb



DEVICE

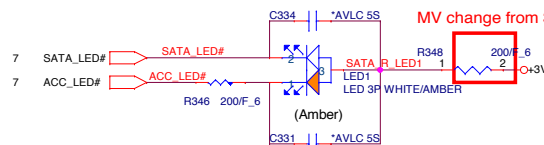
Ca

Cb

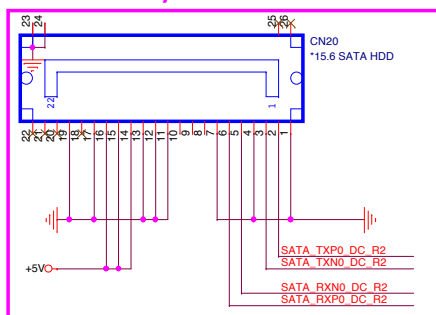
SATA re-driver IC
stuff Rb,Cb , unstuff Ra,Caunstuff SATA re-driver IC
stuff Ra,Ca , unstuff Rb,Cb

SATA LED

MV change from 39ohm to 200ohm for ID



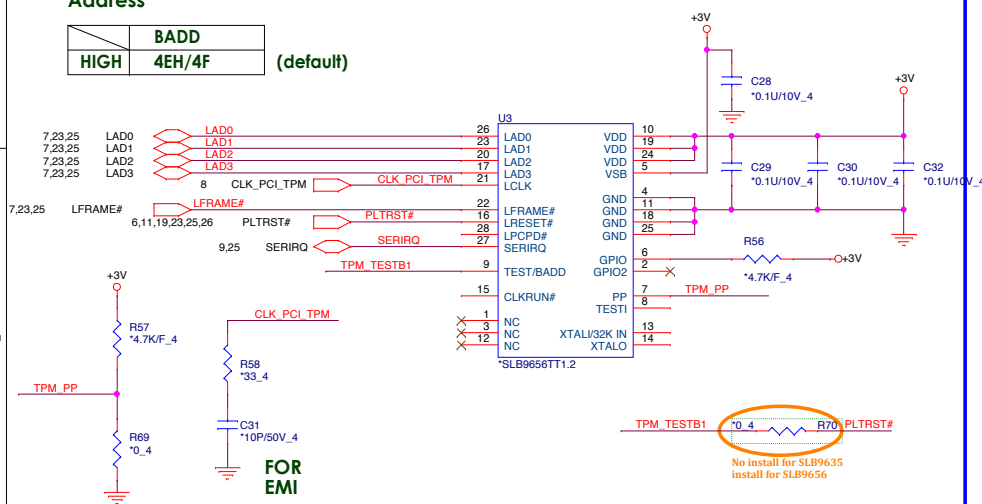
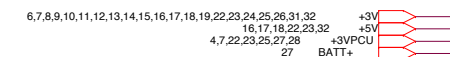
SI-co-lay SATA HDD Connector



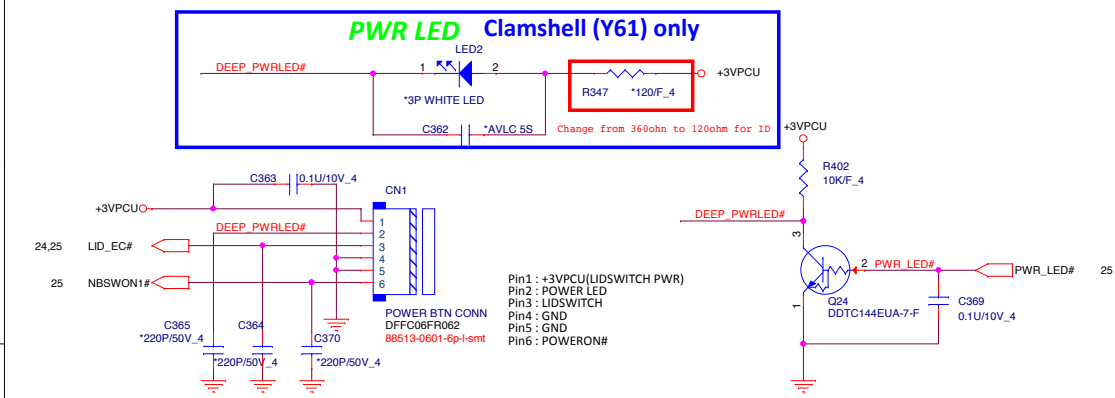
TPM (1.2)

Address

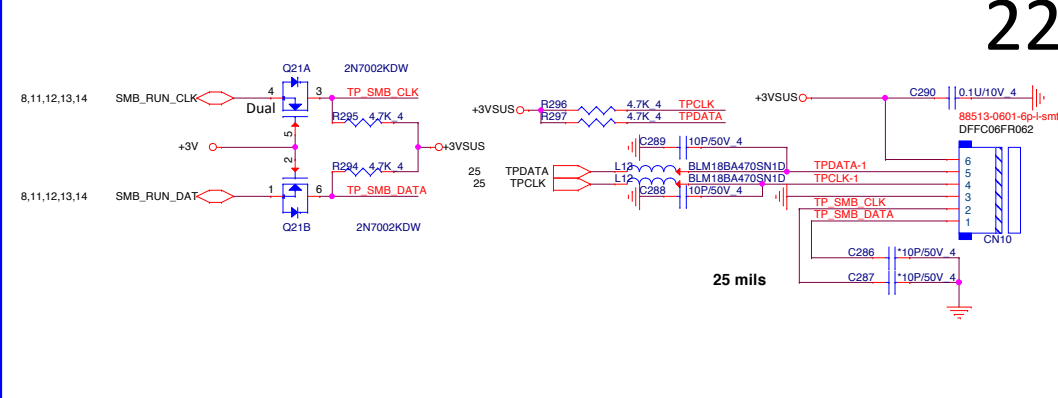
Address	BADD
HIGH	4EH/4F (default)

No install for SLB9635
install for SLB9656

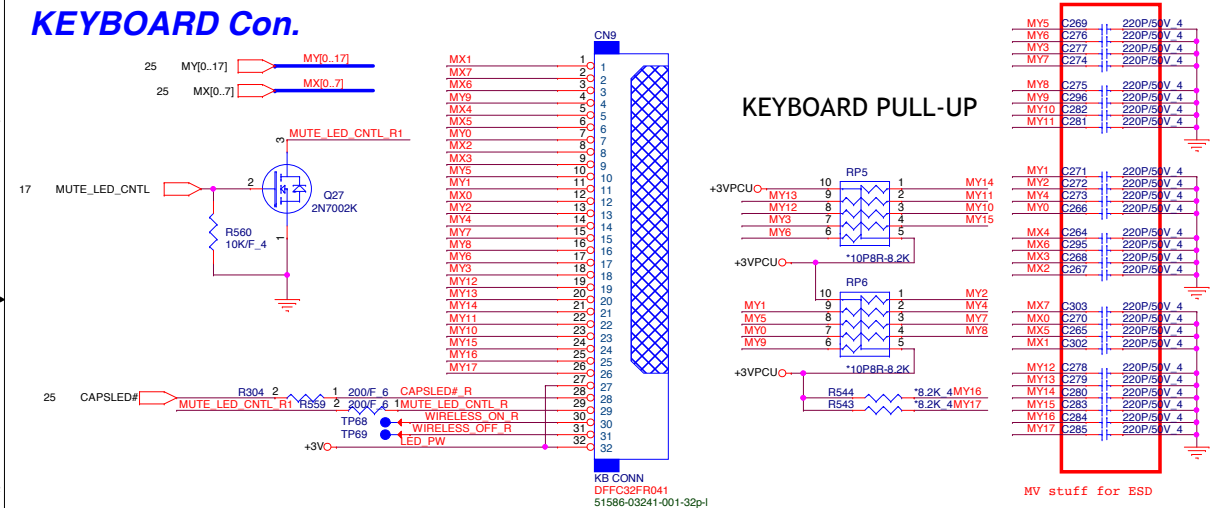
Power Button Connector



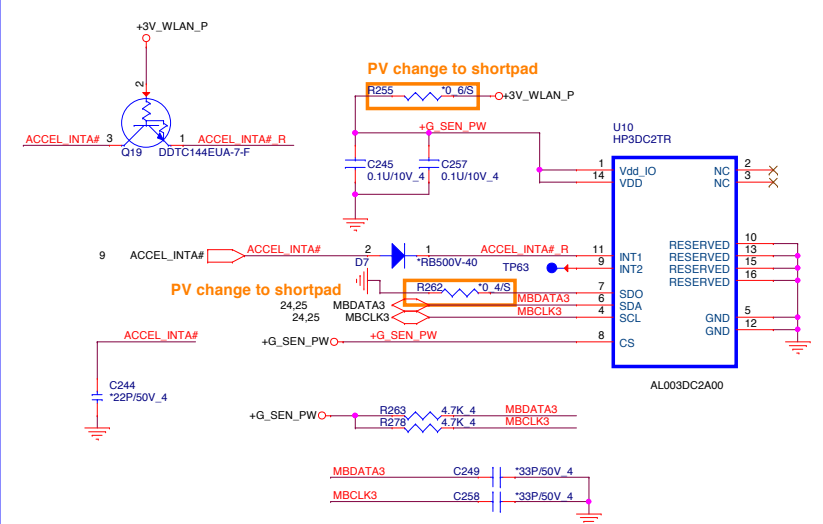
Touch Pad Connector



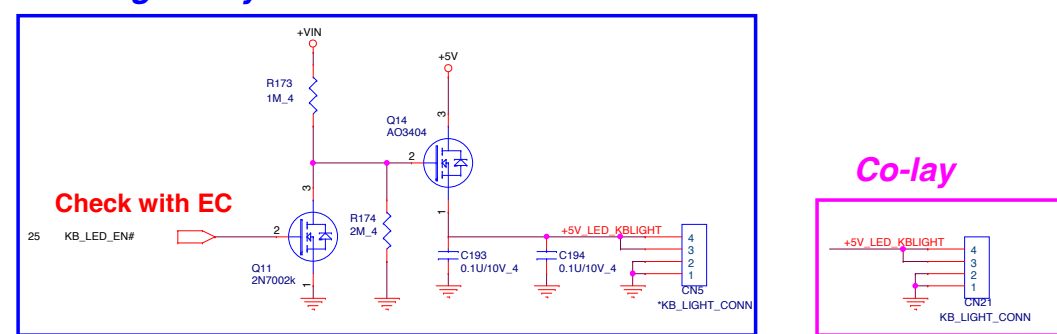
KEYBOARD Con.

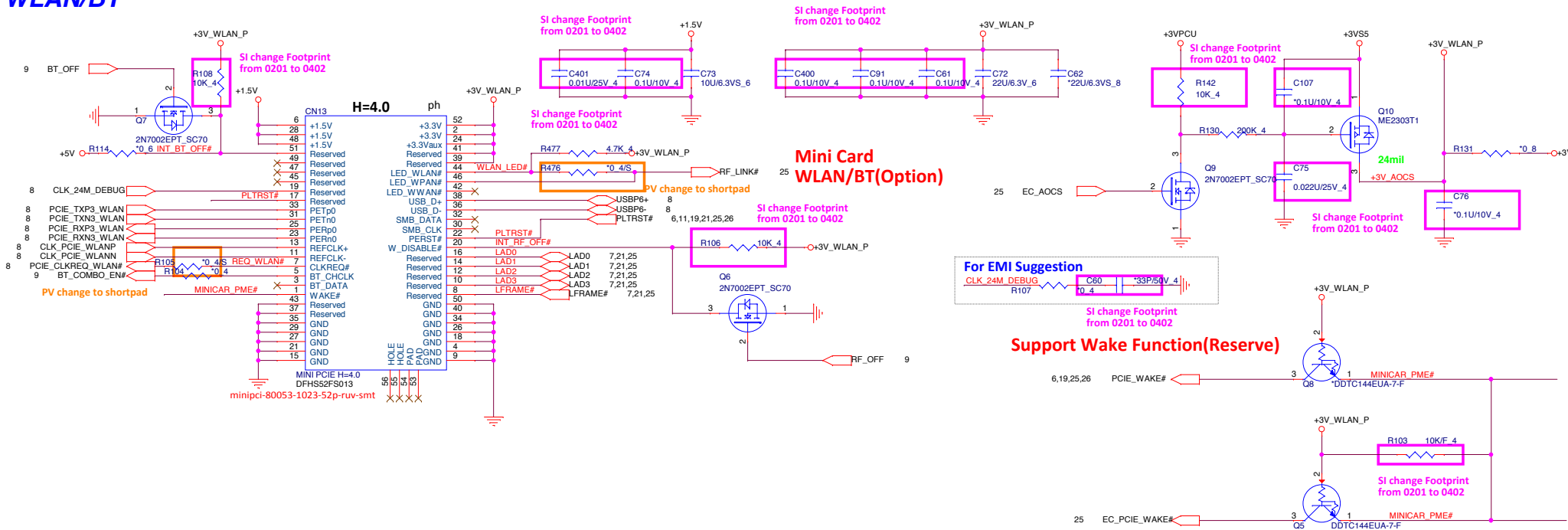


Accelerometer Sensor

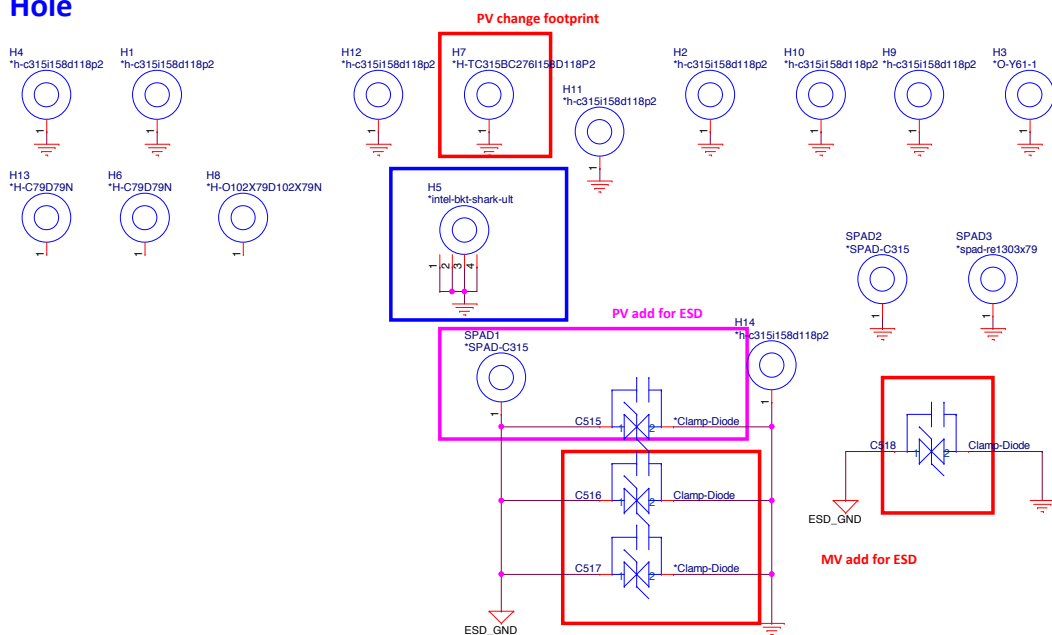


15" KB backlight only





Hole



27 +PRWSRC
6,7,8,9,10,11,12,13,14,15,16,17,18,19,21,22,24,25,26,31,32 +3V
16,17,18,21,22,32 +5V
4,7,22,25,27,28 +3VPCU

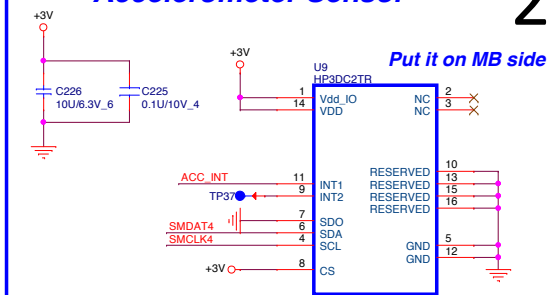


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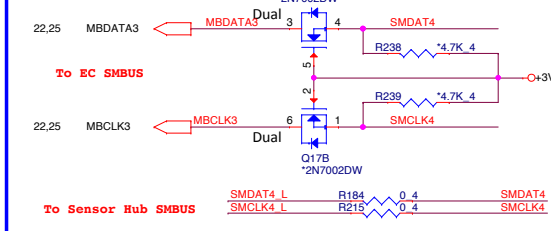
Size Custom	Document Number WLAN/G-Sensor/G-CLK/TS	Rev 1A
Date: Monday, April 21, 2014	Sheet 23 of	32

Accelerometer Sensor

Put it on MB side



Close to U9



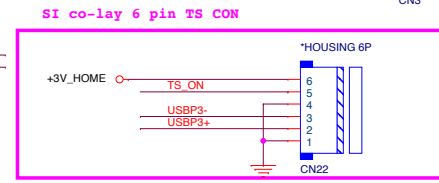
To APU 9 ACCEL_INTH# R488 '0.4 ACC_INT

Reserved SMBus channel 0 for debugging & updating FW
Reserved
SMBus channel 4 for connecting the Sensor (G-sensor)

Reserved TX/RX for debugging
if no use ADC function, please pull down to GND
SMINTx for sensor interrupt

GPG2 can't floating
GPG2 Pull High Enable mirror function.
GPG2 Pull Low Disable mirror function.

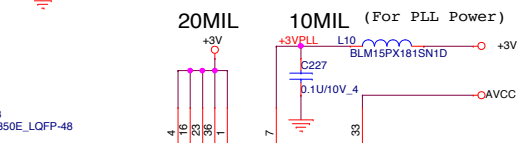
3 IN 1-Sensor
connector to HOME IC



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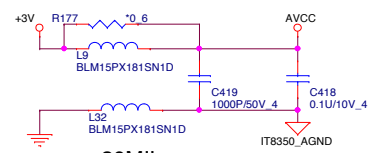
Size Custom	Document Number ITE8350/HP9DS0/HP3DC2	Rev 1A
Date: Monday, April 21, 2014	Sheet 24	of 32

Note: Place all capacitors close to IT8350.

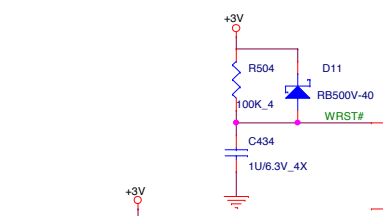


IT8350E LQFP-48

20MIL

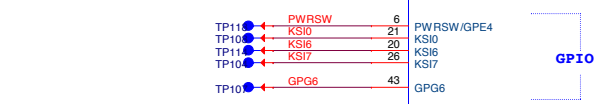


20MIL



USB for Host

SI short L33



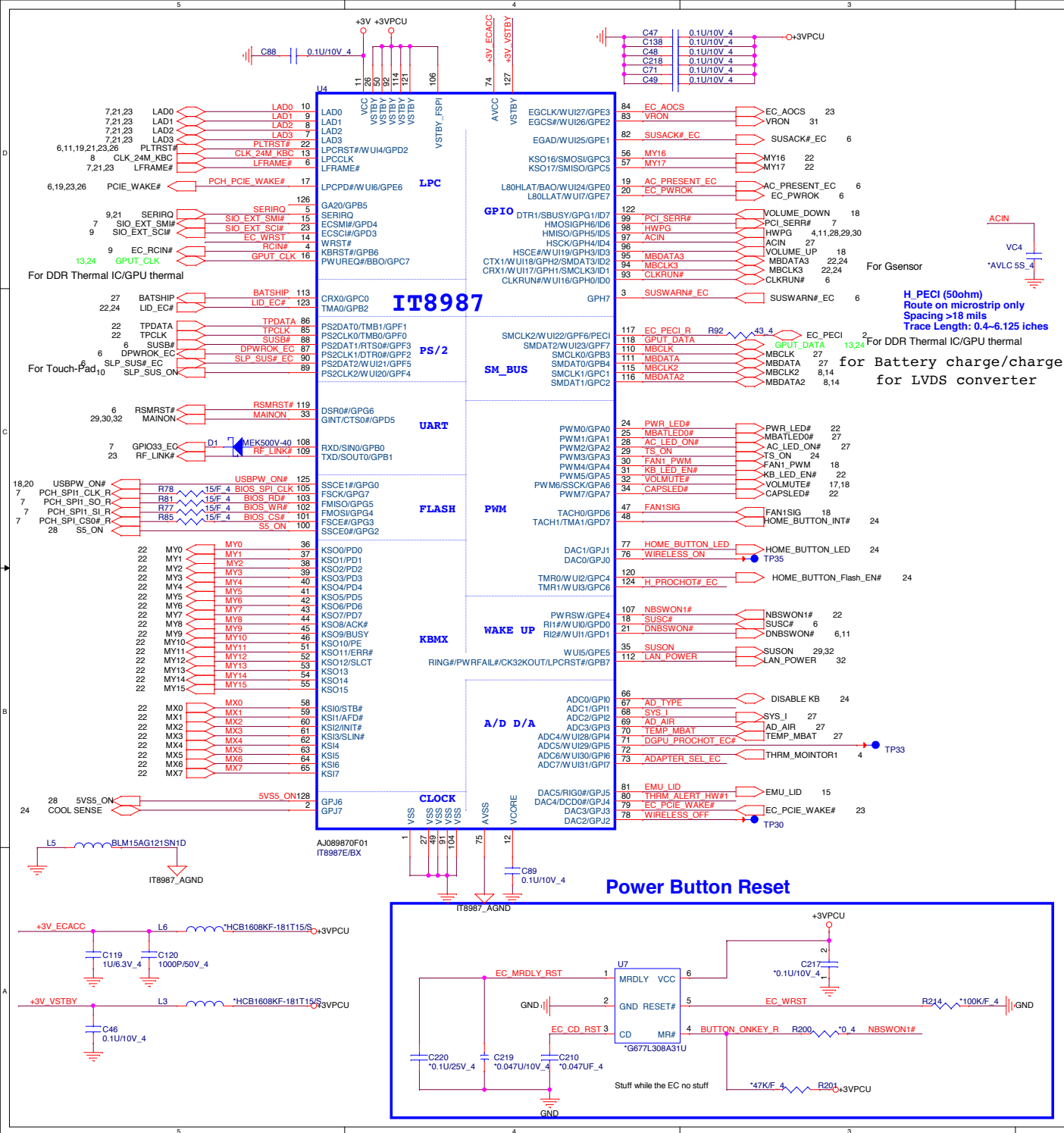
GPIO

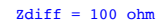
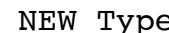
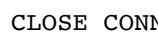


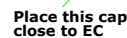
CLOCK

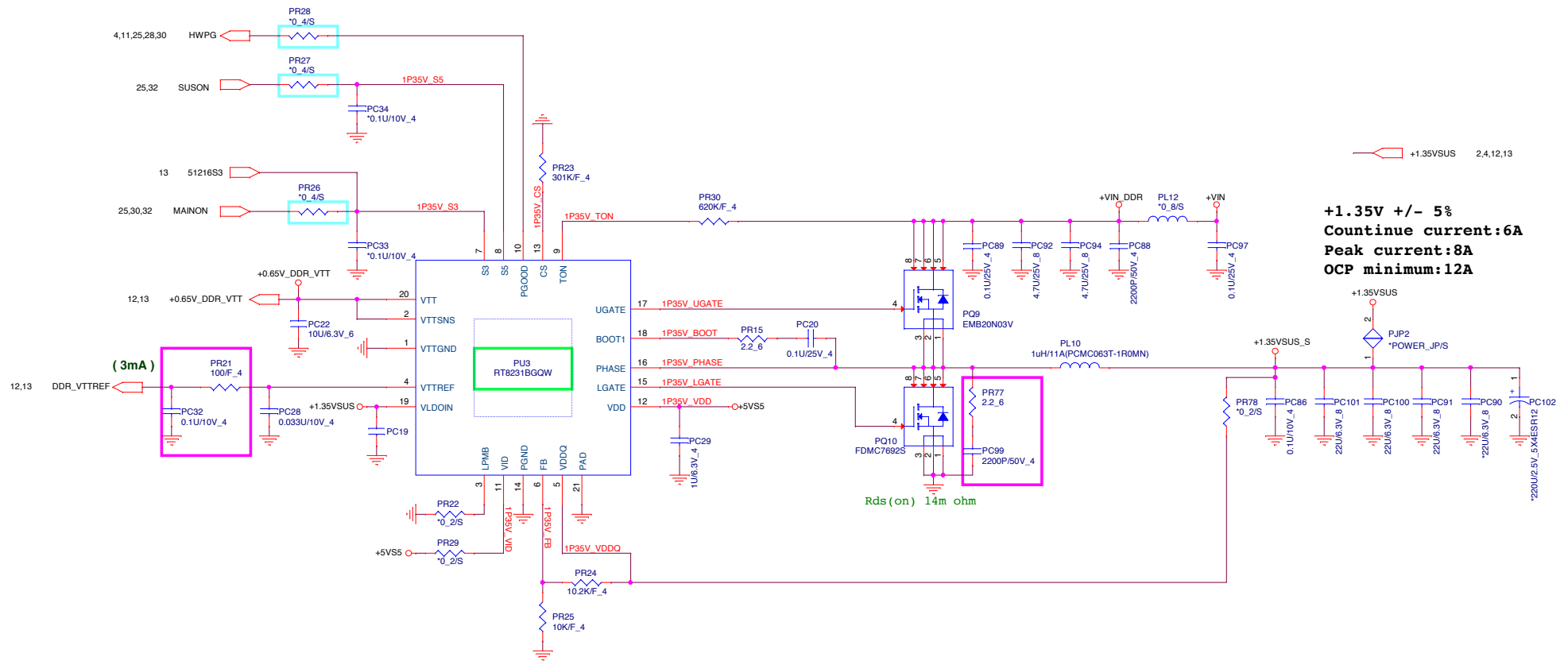


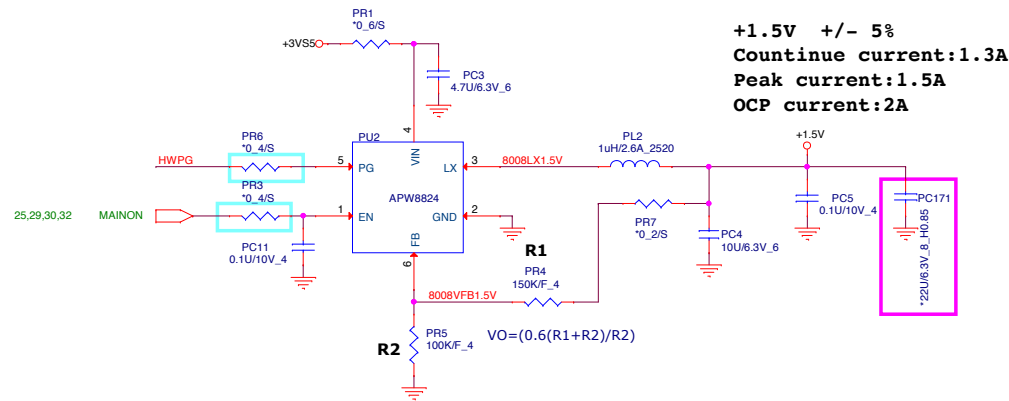
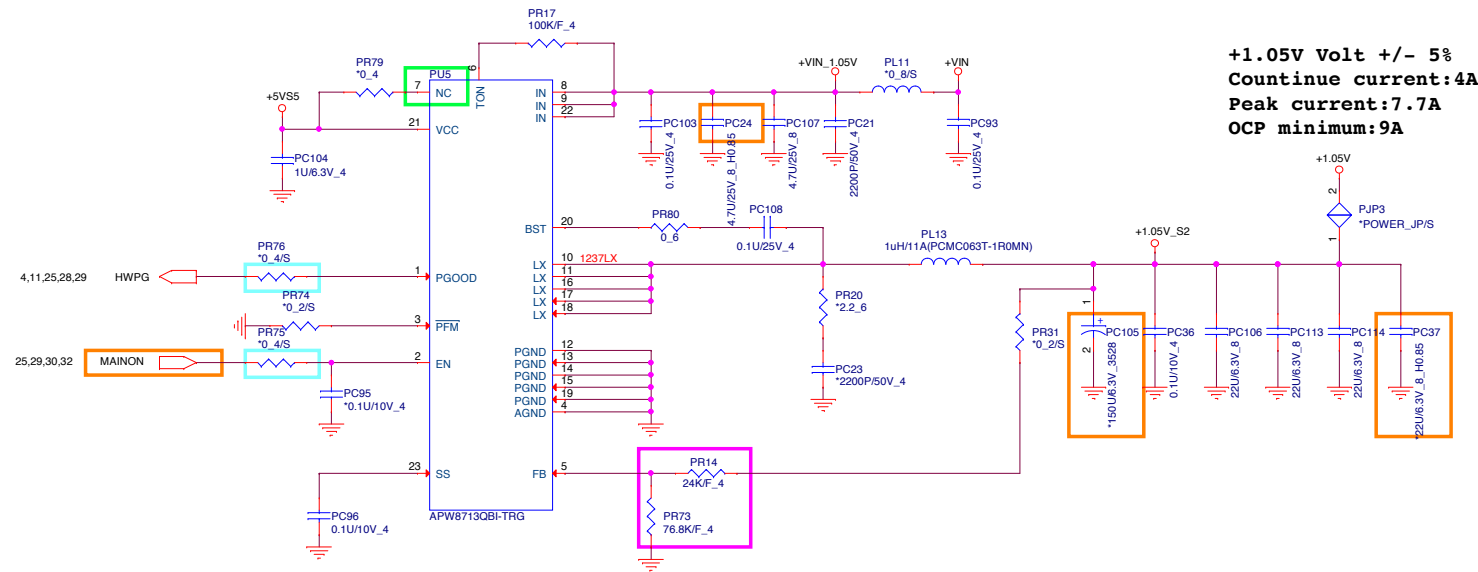
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.



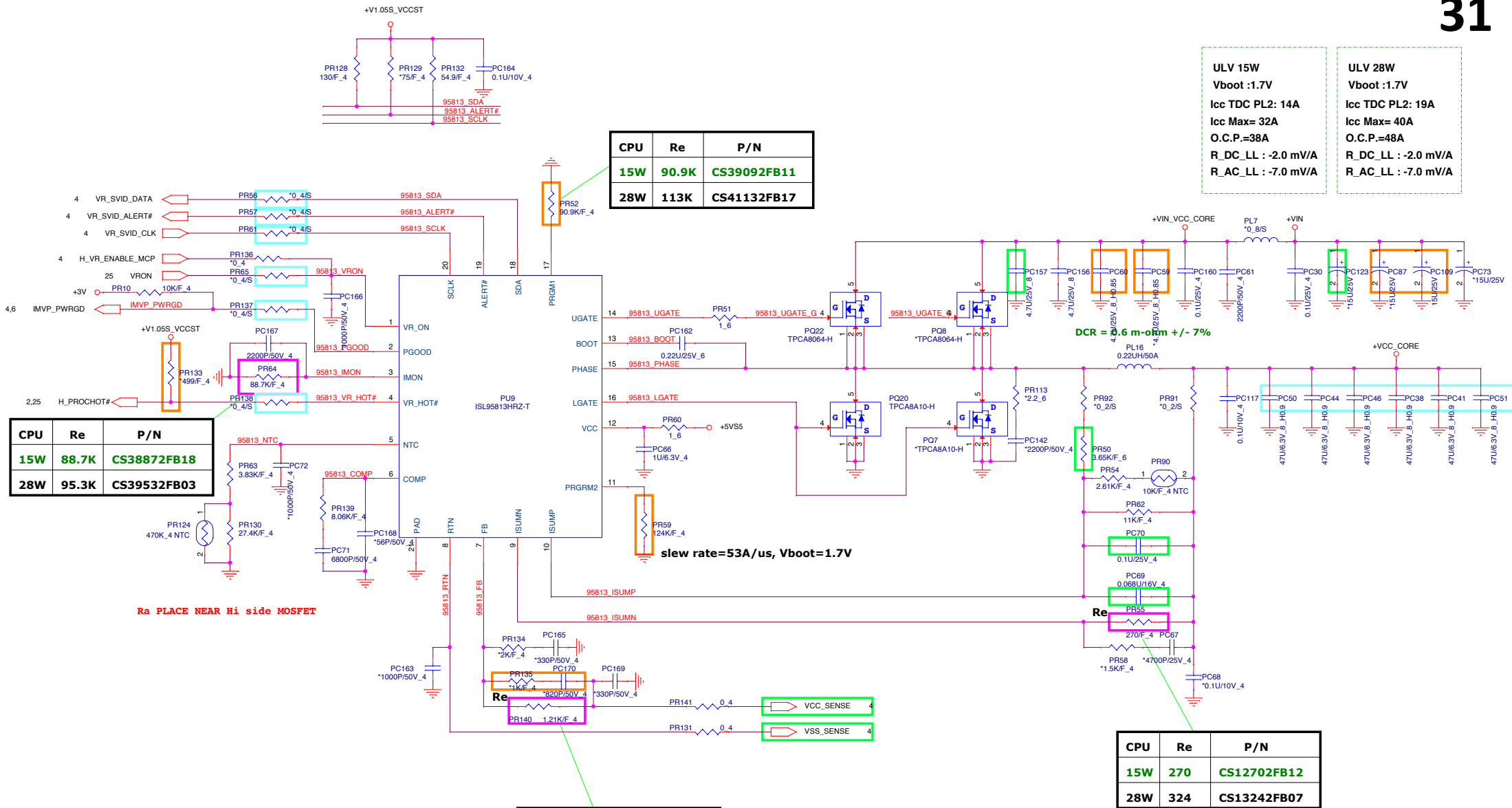
SD / MMC







+VIN 15,22,27,28,29,31,32
+3VSS 6,7,9,10,20,23,24,25,28,32
+5VSS 13,18,20,28,29,31,32
+5VPCU 13,27,28



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Size Document Number Rev
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Date: Monday, April 21, 2014 Sheet 31 of 32

